UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,429	02/16/2000	Takao Toi	Q57908	7134

7590 12/03/2003

Sughrue, Mion, Zinn, MacPeak & Seas
2100 Pennsylvania Avenue N.W.
Washington, DC 20037

EXAMINER	
LAROSE, COLIN M	
ART UNIT	**PAPER NUMBER**
2623	13

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/505,429	TOI, TAKAO	
	Examiner	Art Unit	
	Colin M. LaRose	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 October 2003 has been entered.

Response to Amendments and Arguments

2. Applicant has amended claims 1 and 11 to specify that "all operations necessary to perform said digital image processing and said digital control processing are performed in said field programmable gate array." Applicant then points to the fact that Kolchinsky utilizes two FPGAs (22 and 26, figure 2) as evidence that Kolchinsky does not meet the aforementioned limitation. Examiner disagrees with this assertion.

Kolchinsky clearly discloses the use of two FPGAs, however, Kolchinsky discloses that only one of the two FPGAs, namely the arithmetic unit 26, performs the so-called "digital image" and digital control" processing, as claimed. Column 3, lines 23-29: the address generator 22 selects the address of the image data in the data bank 24 to be sent to the arithmetic unit 26; the image data is subsequently transferred to and processed in the arithmetic unit 26, and then returned to the image data bank 24. Thus, the arithmetic unit 26 performs the digital image and control processing, whereas the address generator 22 merely selects the address of the image data to be processed. Therefore, all operations necessary to perform said digital image processing and

said digital control processing are performed in the arithmetic unit 26; and all operations necessary for performing addressing operations are performed in address generator 22.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-4, 7-10, 11-14, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,486,853 by Baxter et al. ("Baxter") and U.S. Patent 5,301,344 by Kolchinsky.

Regarding claims 1 and 11, Baxter discloses an image processing system (figures 8 and 9), an image processing method of the system comprising:

executing digital image processing of interval of active pixel by processor 66 (figure 8) to perform various functions on pixel data (column 7, lines 18-31: automatic gain control, luminance derivation, etc.);

executing digital control processing according to commands issued during an interval of non-active pixel (i.e. during blanking periods); [Column 7, lines 48-55: control commands are received by processor 70 during blanking period and executed accordingly.]

executing digital image processing again (each line of an image constitutes a different active/non-active region, so digital image processing is repeated for every said region in order to process an entire image).

Baxter is silent to utilizing an FPGA for executing said image and control processing wherein first and second internal logic descriptions, corresponding to each processing, are

written to the FPGA. Instead, Baxter teaches utilizing dedicated processors 66 and 70 for executing each type processing.

Kolchinsky discloses a reconfigurable image processing system (figure 2) that is implemented by FPGAs (22 and 26, figure 2), wherein arithmetic unit 26 is operative to process image data. Kolchinsky teaches that, conventionally, separate image processing operations require separate hardware (column 1, lines 23-24). Baxter, as noted above, requires separate processors (66, figure 8, and 70, figure 9) for image processing and control processing.

Kolchinsky's system uses reconfigurable gate arrays to perform a variety of operations, so that processing algorithms "can be changed easily and quickly without hardware replacement" (column 2, lines 1-2). That is, the image processing functions of multiple dedicated processors such as those taught by Baxter are be performed by a single reconfigurable FPGA (arithmetic unit 26, figure 2) disclosed by Kolchinsky.

With reference to figure 3, first, the command corresponding to the operation to be executed is read from the command file at step 50. Then, the code corresponding to the operation is identified and placed into a register at step 52. Then, the command is executed at step 58 on the condition that proper reconfiguration of internal logic has occurred.

Kolchinsky teaches (figure 4) that both image processing (e.g. image compression, color processing) and control processing (e.g. zooming/panning) are executed by the arithmetic unit 26 (figure 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace Baxter's separate processors 66 and 70 by Kolchinsky's reconfigurable FPGAs to achieve the claimed invention since Kolchinksy provides a much simpler and more hardware-

efficient system for effecting image and control processing. As explained above, Kolchinsky discloses all operations necessary to perform said digital image processing and said digital control processing are performed in a single field programmable gate array -- arithmetic unit 26.

Regarding claims 2 and 12, Baxter teaches there is provided an image pick-up element (CCD 22, figure 9), the system executing color signal processing during active pixel interval and control processing during non-active interval, as addressed above for claim 1.

Regarding claims 3 and 13, Baxter teaches interval of non-active pixel is a VBI (column 7, lines 48-51).

Regarding claims 4, 7, 14, and 17, Baxter does not expressly disclose utilizing the HBI and optical black pixel interval as non-active regions, however, effecting control processing during the HBI and optical black pixel intervals was well-known by those skilled in the art and was a common practice at the time the invention was made.

Regarding claims 8-10 and 18-20 Baxter (column 7, lines 18-31) and Kolchinsky (figure 4) disclose performing white balance, AF, and lightness control processing.

5. Claims 5, 6, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter and Kolchinsky, and further in view of U.S. Patent 5,754,227 by Fukuoka.

Regarding claims 5, 6, 15, and 16, Baxter (column 7, lines 40-43) and Kolchinsky (figure 4) teach executing compression but do not expressly disclose executing control processing, such as code quantity control, in relation to the image compression in the non-active interval.

Fukuoka discloses a camera interface similar to that of Baxter wherein control commands are issued during the non-active interval (column 8, lines 40-43). Fukuoka also teaches performing compression on the active part of the image and teaches that control commands sent during the non-active interval comprise compression parameters, such as a scale factor, or code quantity (column 10, lines 7-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Baxter and Kolchinsky by Fukuoka to achieve the claimed invention since the ability to adjust the compression ratios and scale factors, as taught by Fukuoka, provides control over the compression operations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (703) 306-3489. The examiner can normally be reached Monday through Thursday from 8:00 to 5:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au, can be reached on (703) 308-6604. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (703) 306-0377.

CML

Group Art Unit 2623

1 December 2003

AMELIA M. AU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600